What is claimed is:

1. A binary carry logic circuit receiving an input bit and a carry-in bit to generate a carry-out bit, comprising:

a transfer gate, having a data input and a data output, turned on when said input bit is active, said data input receiving said carry-in bit; and

a transistor, having a current channel connected between a power supply potential and said data output, a logic value of said power supply potential being equal to that of said carry-in bit in an inactive state, turned on when said input bit being inactive;

wherein said carry-out bit is on said data output.

2. A half adder circuit receiving first and second input bits to generate first and second output bits, comprising:

a transfer gate, having a data input and a data output, turned on when said first input bit is active, said data input receiving said second input bit;

a transistor, having a current channel connected between a power supply potential and said data output, a logic value of said power supply potential being equal to that of said second input bit in an inactive state, turned on when said first input bit being inactive; and

a logic circuit, generating said first output bit which is active when either said first or second input bit is active;

wherein said second output bit is on said data output.

112 ③. The half adder circuit of claim 2, wherein said second input is active-low and said power supply potential is a higher one.

112 ④. The half adder circuit of claim 2, wherein said second input is active-high and said power supply potential is a lower one.

5. An incrementer comprising a plurality of half adder circuits each adding a carry-in bit to an input bit to generate an output bit and a carry-out bit, said plurality of half adder circuits being connected in cascade in regard to said carry-in and carry-out bits, each of said half adder circuits other than one for the least significant digit comprising:

a transfer gate, having a data input and a data output, turned on when said input bit is active, said data input receiving said carry-in bit;

a transistor, having a current channel connected between a power supply potential and said data output, a logic value of said power supply potential being equal to that of said carry-in bit in an inactive state, turned on when said input bit being inactive; and

a logic circuit, generating said output bit which is active when either said input bit or said carry-in bit is active;

wherein said carry-out bit is on said data output.

6. The incrementer of claim 5, wherein said half adder circuit for the least significant digit comprises a NAND gate or an AND gate generating a carry-out bit.

7. The incrementer of claim 5, wherein said half adder circuit for the most significant digit further comprises an inverter connected to said data output thereof to shape a waveform of a signal of said carry-out bit.

8. The incrementer of claim 6, wherein said half adder circuit for the most significant digit further comprises an inverter connected to said data output thereof to shape a waveform of a signal of said carry-out bit.

9. A binary borrow logic circuit receiving an input bit and a borrow-in bit to generate a borrow-out bit, comprising:

a transfer gate, having a data input and a data output, turned on when said input bit is inactive, said data input receiving said borrow-in bit; and

a transistor, having a current channel connected between a power supply potential and said data output, a logic value of said power supply potential being equal to that of said borrow-in bit in an inactive state, turned on when said input bit being active;

wherein said borrow-out bit is on said data output.

10. A half adder circuit receiving first and second input

bits to generate first and second output bits, comprising:

a transfer gate, having a data input and a data output, turned on when said first input bit is inactive, said data input receiving said second input bit;

a transistor, having a current channel connected between a power supply potential and said data output, a logic value of said power supply potential being equal to that of said second input bit in an inactive state, turned on when said first input bit being active; and

a logic circuit, generating said first output bit which is active when either said first or second input bit is active;

wherein said second output bit is on said data output.

11. The half adder circuit of claim 10, wherein said second input is active-low and said power supply potential is a higher one.

12. The half adder circuit of claim 10, wherein said second input is active-high and said power supply potential is a lower one.

13. A decrementer comprising a plurality of half subtractor circuits each subtracting a borrow-in bit from an input bit to generate an output bit and a borrow-out bit, said plurality of half subtractor circuits being connected in cascade in regard to said borrow-in and borrow-out bits, each of said half subtractor circuits other than one for the

least significant digit comprising:

a transfer gate, having a data input and a data output, turned on when said input bit is inactive, said data input receiving said borrow-in bit;

a transistor, having a current channel connected between a power supply potential and said data output, a logic value of said power supply potential being equal to that of said borrow-in bit in an inactive state, turned on when said input bit being active; and

a logic circuit, generating said output bit which is active when either said input bit or said borrow-in bit is active;

wherein said borrow-out bit is on said data output.

14. The decrementer of claim 13, wherein said half subtractor circuit for the least significant digit comprises a NAND gate or an AND gate generating a borrow-out bit.

15. The decrementer of claim 13, wherein said half subtractor circuit for the most significant digit further comprises an inverter connected to said data output thereof to shape a waveform of a signal of said borrow-out bit.

16. The decrementer of claim 14, wherein said half subtractor circuit for the most significant digit further comprises an inverter connected to said data output thereof to shape a waveform of a signal of said borrow-out bit.